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Investigation of a New Technique for Adaptive Cancellation of Noise in MOSFET Op. Amps.

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ABSTRACT. The paper presents a new technique for adaptive cancellation of noise in MOSFET IC operational amplifiers. It employs two operational amplifiers, one is passive with its inverting and noninverting inputs short circuited. This operational amplifier is only responsible to amplify its equivalent input noise and to give a proportional output voltage. The second operational amplifier is active and is used to amplify the signal to be processed together with its equivalent input noise and gives, thus, a proportional output voltage. The two operational amplifiers are coupled to each other through a common floating gate so that the noise of the passive amplifier is subtracted from the input of the second one and makes it, therefore, noise-free (~lnV/$\sqrt{\text{Hz}}$ or 0.1 μV_{rms} within 2.5 kHz bandwidth) over a wide variety dynamic range of input voltage (~120 dB) and ambient temperature. A feedback loop is added to improve the amplifier linearity (better than 2%). The standard 2 μm CMOS technology is used for the realization of the proposed noise-free operational amplifier.

1. Introduction

The need for noise-free operational amplifiers for use in many precision applications has recently been greatly increased[1-3]. Numerous studies concerning the specification and evaluation of devices and amplifiers' noise have been developed, in addition to great efforts aiming at compensation or cancellation of this noise[1,3,4,5].

These contributions showed that the most important noise sources are[1,3,5]: a) the 1/f noise resulting from channel and oxide layer activities and, b) the

channel thermal noise. The already-known techniques used to minimize the noise are complicated and considered incapable of efficiently minimizing the noise since these techniques necessitate the employment of an excessive number of devices and circuitries which add to the amplifier noise. The use of these devices and circuitries also inserts new poles which produce appreciable phase shift at high frequencies and represents a serious instability problem. It leads, besides, to greater chip area and power consumption and degrades the amplifier reliability and persistivity[6]. To overcome these problems, exceptionally high speed devices with sophisticated and expensive technology are requested.

We propose a new technique for adaptive cancellation of the high-gain operational amplifier noise (below $1nV/\sqrt{Hz}$ over a very wide dynamic range of signal level (slightly greater than 120 dB) regardless of the ambient temperature variations. It is integrated using the standard 2 μm floating gate MOS technology. It is seen to be free from the majority of drawbacks of all already-known systems. Moreover, it is quite simple, reliable insensitive to device mismatching and has a better linearity (better than 2%) owing to the use of a specially designed voltage controlled resistors used to provide a voltage dependent negative feedback. The study and modelling showed that the noise cancellation is successfully achieved from dc up to high efficiency. Figure (1) shows the schematics of the new technique.

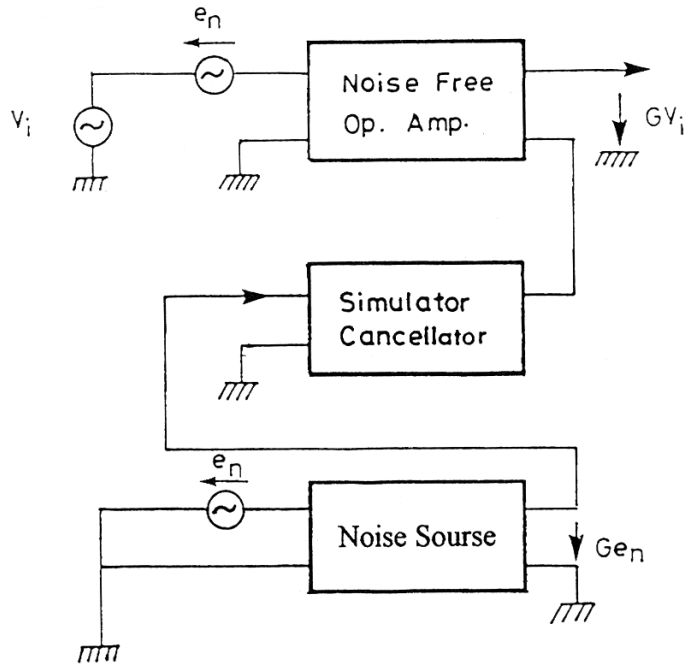

FIG. 1. Technique of cancellation.

$$f = \frac{I_g}{C_{FG} e_n} \sim 10^{14} \text{Hz} \tag{1}$$

With I_g being the hot carrier gate current (~10^{-10} A), C_{FG} the floating-gate to channel capacitance (10^{-16} F), and e_n the equivalent noise voltage to be cancelled (~ln V).

Measurements on an experimental device using the proposed techniques showed excellent agreement with the theory and simulations and indicated a powerful potentiality in noise cancellation over all already-known techniques.

2. Architecture

It is constructed of two basic units. The first is noise simulator which is responsible of simulating the device noise under all the conditions of operation while the second is the noise free active device. Figure (2) shows the corresponding schematics.

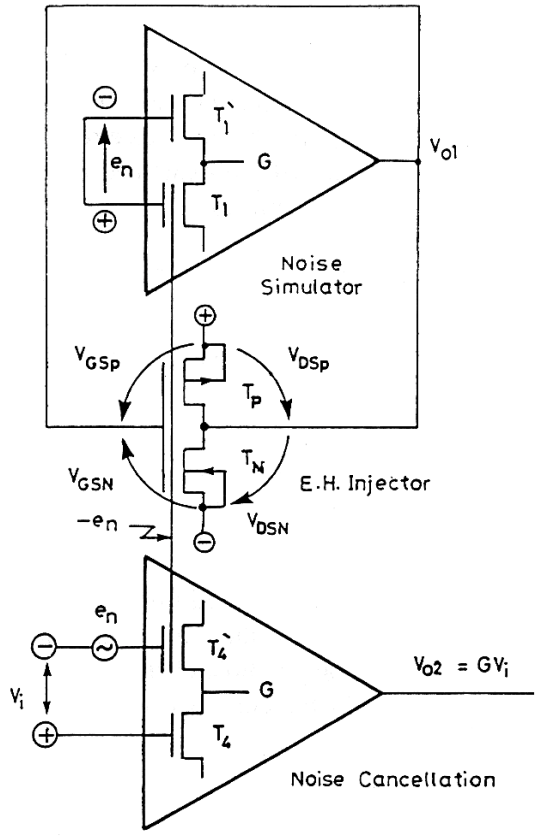

FIG. 2. Schematic of the adaptive noise cancellation.

Each of these building blocks is constructed as shown in Fig. (3,a,b,) of two input driver MOSFET's T_1, T_1' and T_4, T_4' and two current sources T_2, T_2', T_5, T_5' each pair of driver/source string T_1, T_2, T_1' , T_2' and T_4, T_5, T_4', T_5' are connected in different configuration with a common mode negative feedback through T_3 and T_6, respectively, to stabilize the currents and node voltages against any device mismatching, characteristics spreading, aging and/or temperature excursions.

These two units are fabricated and realized on the same chip, using the 2μ m trapezoidal FG-CMOS technology (see Fig. (4-a)), with so compact layout which keeps the physical separation between T_1, T_1' and T_2, T_2' smaller than 50 μm. This guarantees the maximum possible device to device matching and fulfil the best device identity. In this case, any shift or excursion in the T_1, T_1' parameters will be equal and identical to that occurring in the parameters of T_2, T_2'. Better device matching can be achieved as will be shown by interdigitating T_1 with T_2 and T_1' with T_2' as shown in Fig. (4-b).

A third unit, the electron hole EH injector, is inserted and used to follow the variations of the first device noise, simulate it and transfer it to the floating gate of the inverting input driver MOSFET T_4. It is constructed of a P-channel MOSFET J_P which is responsible of injecting holes into the common floating gate and an N-channel MOSFET J_n which injects electrons into the floating gate according to the polarity of V_{01} as will be explained below. Fig. (5) shows a cross section and the layout of the EH injector.

3. Mechanism of Operation

The mechanism of noise simulation is as follows: suppose that the operational amplifier input equivalent noise is e_n. Then the output V_{01} of the operational amplifier noise simulator is $V_{01} = -Ge_n$ with G being the amplifier gain. The negative voltage V_{01} is transferred simultaneously to the common drain of the EH injector. This makes the gate source voltage V_{GSP} of the MOSFET T_p negative and makes its drain to source voltage V_{DSP} to be sufficiently high that hole heating takes place in its channel[8,9]. These hot holes being energetic become capable of jumping over the Si-SiO_2 interface potential barrier and penetrating into the SiO_2 layer where they are accelerated towards the floating gate by the gate-voltage induced oxide field where they are falling in trapping inside the floating gate potential well. The trapped hole charge makes the floating gate to attain a positive potential V_{FG} which increases with time according to the equation.

$$V_{FG}(t) = \frac{I_{gp}t}{C_{FG}} \sim 10^6 t \qquad (2)$$

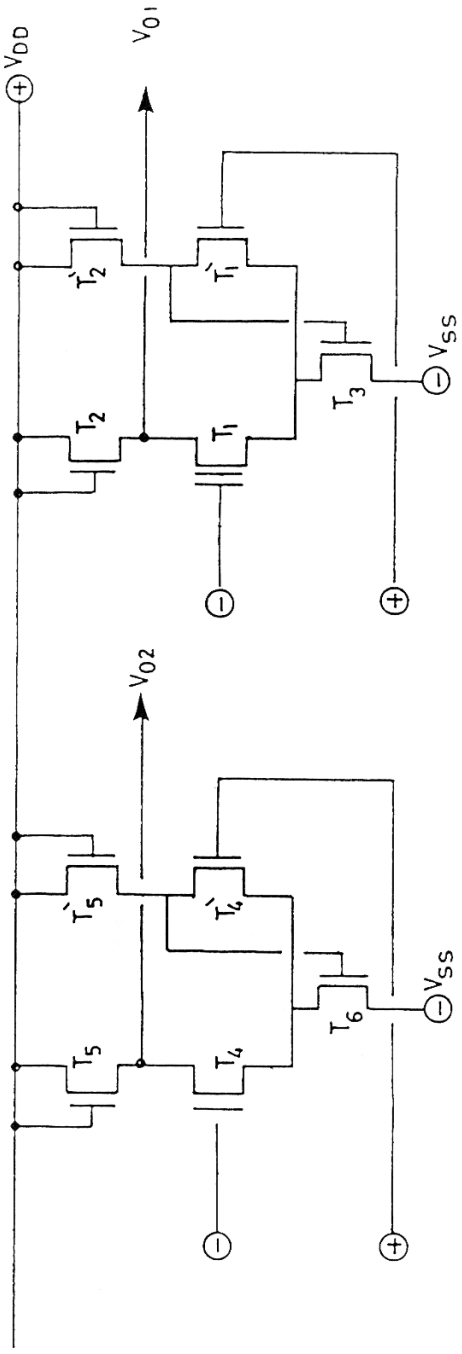

FIG. 3. The passive and active op. amps.

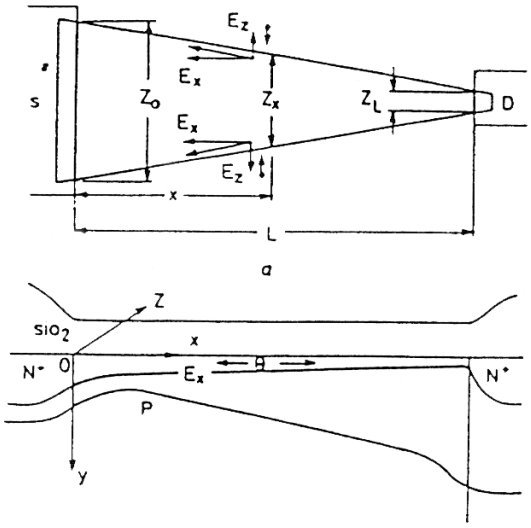

FIG. 4a. TG-MOSFET structure.

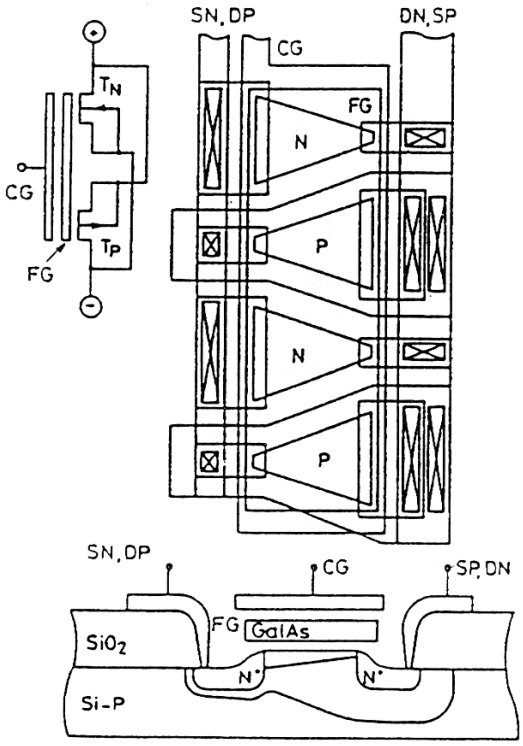

FIG. 4b. TG-MOSFET inter digitation.

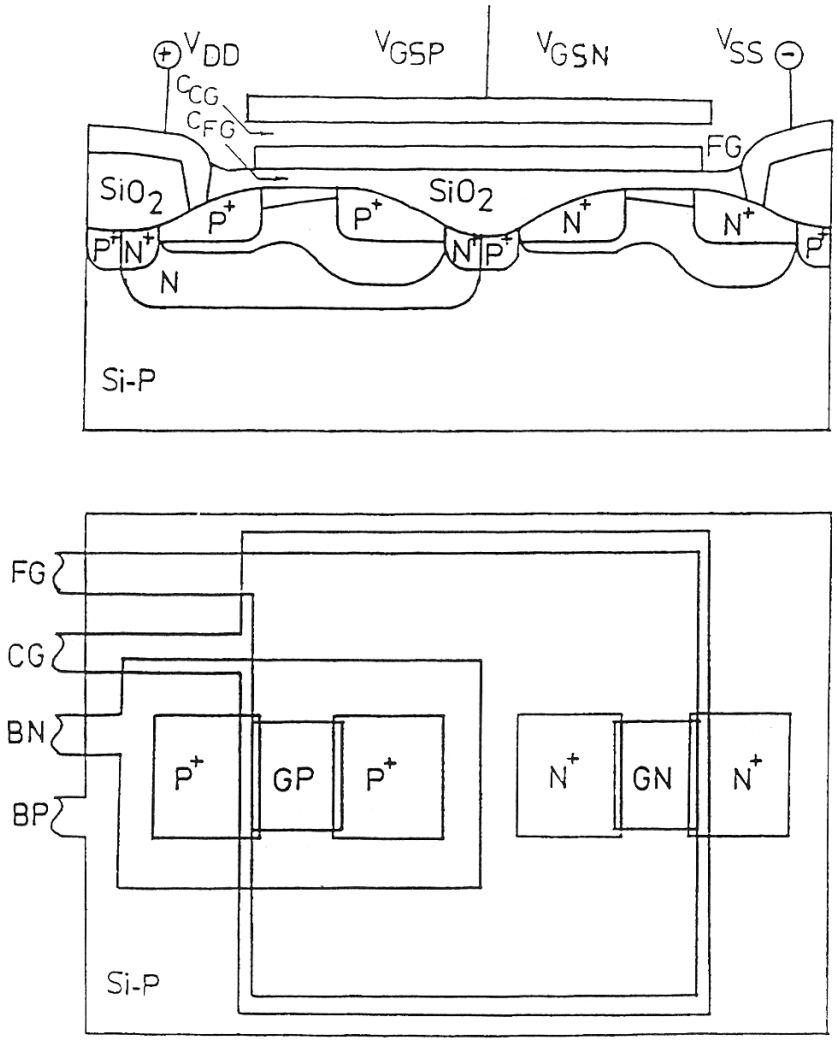

FIG. 5. A cross section and layout of MOSFET.

Where

I_{gp} is the hot hole gate current ($\sim 10^{-10}$ A)

C_{FG} is the floating gate to the channel capacitance ($\sim 10^{-16}$ F/um^2)

V_{FG} increases with time, when it becomes equal to e_n after t given by:

$$t = \frac{e_n}{10^6}\,\text{sec} \approx 10^{-15}\,\text{sec.}\ ;\ e_n \approx 10^{-9}\,\text{V} \tag{3}$$

This V_{FG} variation is directly transferred to the noise simulator input and makes V_{01} drop to zero and hence turns T_P off which stops the flow of I_{gp} and enables the EH injector to latch up the noise voltage e_n. It is seen from equation (3) that the speed of response of the EH injector can be as high as 1 V/μ sec which enables the EH injector to follow any fast variation in the device 1/f (up t some GHz). However larger 1/f noise levels which need longer coverage time will also be successfully cancelled because the EH injector is still much faster. To increase further the cancellation rate, the known rectangular gate MOSFET is replaced by the trapezoidal gate MOSFET[8,10] shown in Fig. (4-a). Interdigitation of the T_1, T'_1 and T_2, T'_2 gates (see Fig. (4-b)) enhances the device matching and allows more powerful noise cancellation.

When e_n reverses its polarity due to operating conditions effects, V_{01} reverses its polarity as well. In this case the electron injector T_N will be turned on (V_{GSN} will be positive) and its drain to source voltage heats up the channel electrons which will be injected into the oxide layer and accelerated into the floating gate where they will be trapped and make V_{FG} to attain a negative value equal to e_n after the t defined by equation (3) this voltage variation being transferred to the noise simulator input, makes V_{01} to go to zero. T_N is turned, therefore, off and the flow of I_{gn} is stopped which enables the EH injector to latch up the noise voltage e_n during its stokastic variations.

When e_n is zero (I/f noise is completely cancelled), the two injectors T_P and T_N turn on and V_{DSP} and V_{DSN} are so that electron and hole heating occur simultaneously, which leads to two equal electron and hole gate currents I_{gp} and I_{gn}. In this case the net charge accumulation in the floating gate is zero and V_{FG} remains zero.

The latch up phenomenon characterizing the T_P, T_N inverter circuit configuration makes V_{01} to have also a very high speed of response (about 10^3 V/μ sec or 10^3 times faster than the required rate for successful noise cancellation) which enhances adaptivity of the noise cancellation.

4. Experimental and Simulation Results

The channel current I_{DS} and the hot carrier gate current I_g are first measured versus V_{GS} at different values of V_{DS} for different device geometries. Figure

(6) shows the experimental setup used to perform the measurements. From these measurements the values of the channel and oxide transconductances g_{mD}, g_{mox} and their dependence on the device biasing conditions and geometry are specified. The drain and gate currents can be formulated by[4-7].

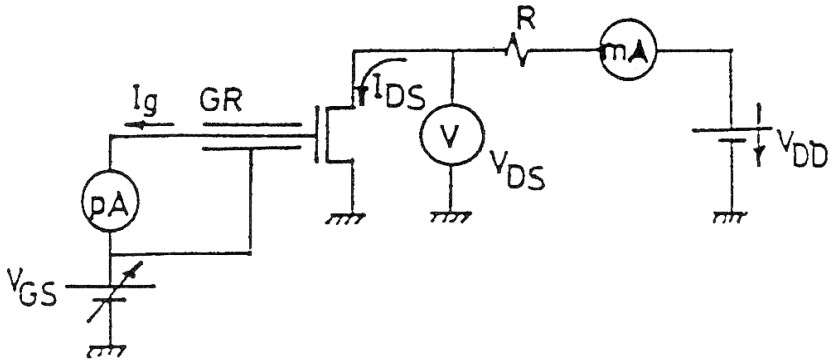

FIG. 6. Experimental setup.

$$I_{DS} = C_{10}\mu\frac{Z}{L}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \tag{4}$$

$$I_{gn} = \frac{ZL\mu_{0xn}C_0}{d\varphi}[V_{GS} - V_T - \frac{1}{L} - \int_O^L V_x dx][1 - \sqrt{\frac{\varphi_B}{\varepsilon_m}}].$$

$$\exp[-(\frac{\varphi_B}{KT_0} + \frac{d_0}{1_r} + \frac{\lambda}{1_{0x}})] \tag{5}$$

From which the channel and oxide transconductances g_{mD} and g_{mox} can be formulated by:

$$g_{md} = C\ \mu\frac{Z}{L}V_{DS}\ ;\ V_{DS} < V_{DSS} \tag{6}$$

$$g_{mox} = \frac{Z(L - \Delta 1)\mu_{oxn}}{d_o\lambda_{ox}}[2V_{GS} - V_T - \frac{1}{L}\int_o^L V_x dx][1 - \sqrt{\frac{\varphi_B}{\varepsilon_m}}]$$

$$\exp[-(\frac{\varphi_B}{KT_0} + \frac{d_0}{1_r} = \frac{\lambda}{1_{0X}}0] \quad ; \quad V_{DS} < V_{DSS} \tag{7}$$

Where Z, L are the channel width and length respectively. (μm)

- μ is the carrier nobility (cm^2/V. sec)
- C_O is the oxide capacitance per unit area (F/m^2)

l_{ox} is the carrier mean ρ_{vce} symbol path in SiO_2 (Aº)
l_r is the carrier mean free path in Si (Aº)
φ_B is the Si-SiO_2 potential barrier (eV)
d_o is the channel depth (Aº)
λ is the Si-SiO_2 potential barrier shift (Aº)
Δl is the pinch off region length (Aº)

Next the equivalent input noise spectrum S_{vg} is measured as a function of V_{GS}. The equivalent channel and gate currents noise spectra S_{I_D} and S_{I_g} can, therefore, be determined from the $g_{mD}\ S_{vg}$ and $g_{mox}\ S_{vg}$ product.

We have measured the equivalent input noise spectra S_{vg} and the resultant channel and the gate current noise spectra S_{I_D} and S_{I_g} for MOSFETs biased in the ohmic region with and without noise cancellations. They are composed of 1/f and $1/f^n$ noise components. We observed that the measured without cancellation. These measurements can be employed to detect the long and short term stressing effects on the short channel MOSFETs high gain operational amplifiers. Figures (7, 8 and, 9) show the evolution of S_{vg}, S_{I_D} and S_{I_g} with frequency and the effect of cancellation on the noise level .

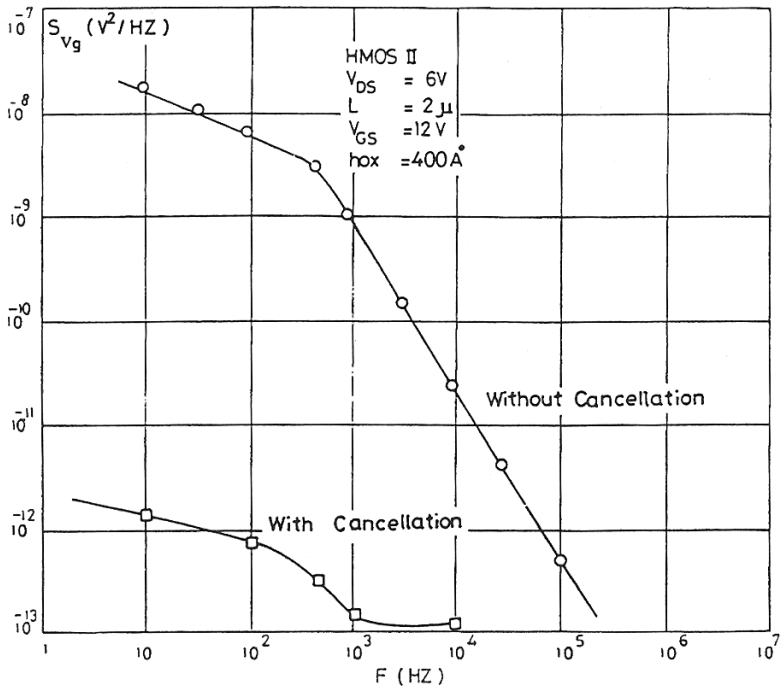

FIG. 7. Gate voltage noise spectrum.

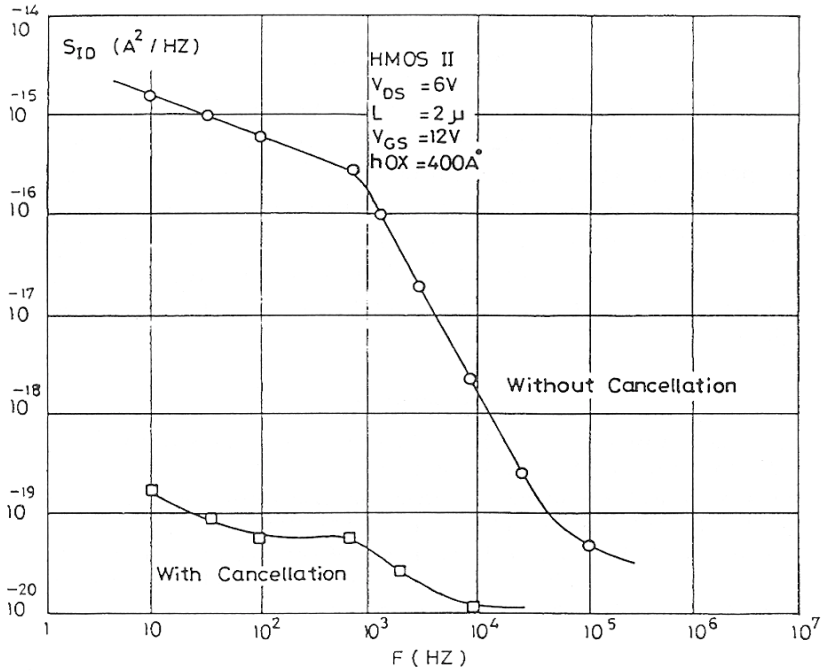

FIG. 8. Channel current noise spectrum.

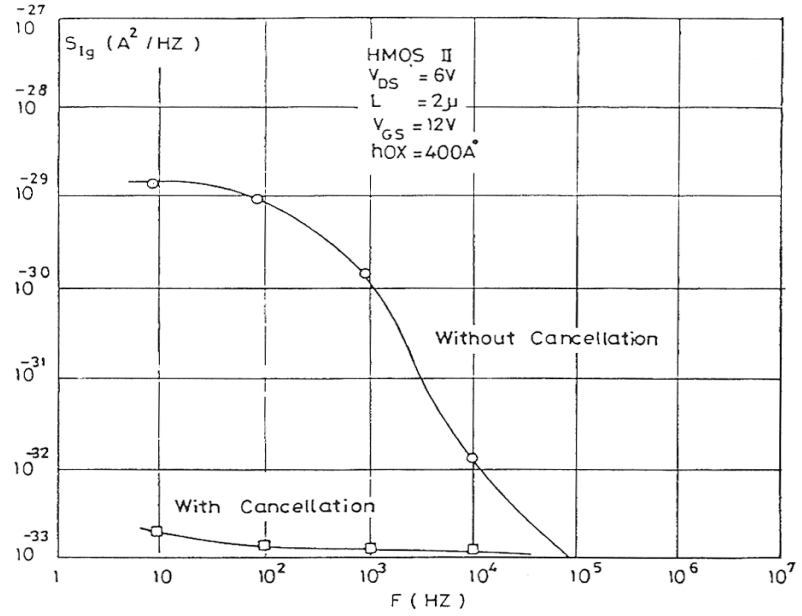

FIG. 9. Hot-carrier gate current noise spectrum.

5. Conclusions

This paper presents and explains a new technique, based on modifying the device construction, for the adaptive cancellation of noise in the high gain MOSFET operational amplifiers. It allows to realize submicronic MOSFET operational amplifiers without fearing from noise increase cause due to the device scaling down. The proposed technique possesses an excellent potentiality in noise cancellation (from frequencies as low as some cycles per second up to very high frequencies; GHz). It helps in fact to reduce the noise level by about four decades.

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دراسة وتبيان تجريبي لتقنية جديدة للإلغاء المتوائم للضوضاء في المكبرات التشغيلية عالية التكبير والمصنوعة بتكنولوجيا م و س

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المستخلص . يعرض هذا البحث بالدراسة والقياسات تقنية جديدة للإلغاء المتوائم للضوضاء في المكبرات التشغيلية عالية التكبير والمصنوعة بتكنولوجيا م و س . وتستخدم هذه الطريقة مكبرين – الأول خامل ويستخدم فقط لإعطاء جهد خروج مناظر لتكبير الضوضاء فيه ، والثاني نشط ويعطي جهد خروج مناظر للضوضاء والإشارة المراد تكبيرها . ويستخدم جهد خروج الأول لإزالة الضوضاء من جهد خروج الثاني عن طريق دائرة تغذية خلفية خاصة . وتتميز هذه التقنية بقدرة عالية على الإلغاء المتوائم للضوضاء مهما تغيرت ظروف التشغيل ، ولقد ساعدت هذه التقنية على تقليل مستوى الضوضاء بما لايقل عن 10^{4} من المرات .